

PATENT



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Larry D. Kinsman et al.

Serial No.: Not Yet Assigned

Filed: July 30, 2001

For: METHOD FOR FABRICATING A CHIP
SCALE PACKAGE USING WAFER LEVEL
PROCESSING AND DEVICES RESULTING
THEREFROM

Examiner: Unknown

Group Art Unit: Unknown

Attorney Docket No.: 3572.1US (97-1243.1)

NOTICE OF EXPRESS MAILING

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INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
Washington, D.C. 20231

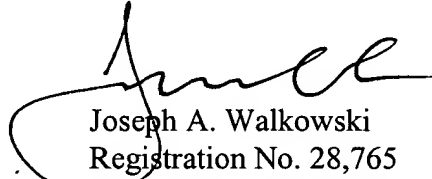
Sir:

The present application is a divisional of application Serial No. 09/586,243, filed June 2, 2000, pending.

Pursuant to M.P.E.P. 2001.06(b), the Examiner is respectfully requested to consider the information of record in the prior application, and to confirm in the first Office Action on the merits that such art has in fact been reviewed. A PTO-1449 form listing all of the information of record in the prior application is enclosed herewith.

This Information Disclosure Statement is filed within three (3) months of the filing date of the above-identified application, and no certification pursuant to 37 C.F.R. § 1.97(c) or a fee pursuant to 37 C.F.R. 1.17(p) is required.

Respectfully submitted,



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Date: July 30, 2001

JAW/ps:dlm

Enclosure: Form PTO-1449

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